UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,748	02/16/2000	Raj Kumar Singh	RAL9-99-0181	6579

25299 7590 12/18/2002

IBM CORPORATION
PO BOX 12195
DEPT 9CCA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER
THANGAVELU, KANDASAMY

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/505,748	SINGH ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-12 of the application have been examined.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statement filed on February 16, 2000 together with copies of the patents and papers. The patents and papers have been considered in reviewing the claims.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

The draft person has objected to the drawings; see a copy of Form PTO-948 for an explanation.

Specification

4. The disclosure is objected to because of the following informalities:

Page 5, Lines 10-11, "2488.32 Gbps (OC-48)" is incorrect.

Page 14, Lines 16-17, "the invention has described with respect to the specific embodiment" is grammatically incorrect.

Appropriate corrections are required.

Claim Objections

5. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

Claims 1-12 are objected to because of the following informalities:

Claim 1, Lines 11-12, "and which provide testing" is incorrect.

Claim 1, Lines 12-13 the statement "testing with multiple vendors of Framers" is incorrect. The statement "testing with Framers from multiple vendors" is correct.

Claim 2, Line 2, "provides Receiver and one Transmit interface" is incorrect.

Claim 4, Lines 2-3, "due to constrains stemming from" is incorrect.

Claim 7, Lines 5-6, "the behavioral model that offer" is grammatically incorrect.

Claim 7, Lines 10-11, "and which provide testing" is incorrect.

Claim 7, Lines 11-12 the statement "testing with multiple vendors of Framers" is incorrect. The statement "testing with Framers from multiple vendors" is correct.

Claim 8, Lines 3-4, "provides Receiver and one Transmit interface" is incorrect.

Claim 9, Line 2, "SONET in interfaces" is incorrect.

Claim 10, Lines 2-3, "due to constraint stemming from" is incorrect.

Claims objected to but not specifically addressed are objected to based on their dependency to an objected claim.

Appropriate corrections are required.

Claim Interpretations

6. The following interpretations are used in the art rejections.

In Claim 1, Lines 12-13 the statement "testing with multiple vendors of Framers" is interpreted as "testing with Framers from multiple vendors".

In Claim 7, Lines 11-12 the statement "testing with multiple vendors of Framers" is interpreted as "testing with Framers from multiple vendors".

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1, 3-5, 7 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kim et al (KI)** (IEEE, August 1999) in view of **Rostoker et al. (RO)** (U.S. Patent 6,470,482), and further in view of **Koziotis et al. (KO)** (IEEE, October 1999).

9.1 **KI** teaches Design and simulation of three ATM ASICs. Specifically, as per claim 1, **KI** teaches a computer based system employing a customizable simulation model of an ATM/SONET framer, for system level verification and performance characterization (Page 25, Col 1, Para 2 and 3; Fig. 1; Page 26, Col 1, Para 4).

KI teaches the computer based system comprising means for developing an accurate customizable model that offer sufficient parameters which can be programmed to represent framers from different vendors (Page 26, Col 1, Para 3). **KI** does not expressly teach the computer based system comprising means for developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent framers from different vendors. **RO** teaches the computer based system comprising means for developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent framers from different vendors (Abstract; Col 7, Lines 22-34), as behavioral models provide simplified model of extremely complicated devices (Col 4, Lines 19-21) and a very complete and accurate description of performance of the modeled device (Col 4, Lines 29-31). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** with the computer based system of **RO** that included means for developing an accurate customizable behavioral model

that offer sufficient parameters which can be programmed to represent framers from different vendors, as behavioral models would provide simplified model of extremely complicated devices and a very complete and accurate description of performance of the modeled device.

KI does not expressly teach the computer based system comprising means for providing two independently configurable components, a receiver and a transmitter, and which provide for testing with Framers from multiple vendors, by changing programmable parameters of the model. **KO** teaches the computer based system comprising means for providing two independently configurable components, a receiver and a transmitter, and which provide for testing with Framers from multiple vendors, by changing programmable parameters of the model (Fig. 1; Table 1), as all communications between the ATM and the SONET have a transmit path and a receive path (Page 1833,Col 1, Para 2 and 4). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** with the computer based system of **KO** that included means for providing two independently configurable components, a receiver and a transmitter, and which provide for testing with Framers from multiple vendors, by changing programmable parameters of the model, as all communications between the ATM and the SONET have a transmit path and a receive path.

9.2 As per Claim 3, **KI, RO** and **KO** teach the system of Claim 1. **KI** and **RO** do not expressly teach that the ATM and the SONET interfaces operate on different clock frequencies and represent two distinct clock domains, and the data interchange between the two the clock domains is achieved by means of FIFO buffer elements and associated control and status signals.

KO teaches that the ATM and the SONET interfaces operate on different clock frequencies and represent two distinct clock domains, and the data interchange between the two the clock domains is achieved by means of FIFO buffer elements and associated control and status signals (Page 1833,Col 1, Para 2; Col 2, Para 3; Fig 1; Page 1834,Col 1, Table 1), as that allows burst read and write independently of external speed and the FIFO provide for speed adaptation and minimize the latency (**KI:** Page 25,Col 2, Para4 to Page 26, Col 1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** and **RO** with the computer based system of **KO** that included the ATM and the SONET interfaces operating on different clock frequencies and representing two distinct clock domains, and the data interchange between the two the clock domains being achieved by means of FIFO buffer elements and associated control and status signals, as that would allow burst read and write independently of external speed and the FIFO would provide for speed adaptation and minimize the latency.

9.3 As per Claim 4, **KI, RO** and **KO** teach the system of Claim 1. **KI** and **KO** do not expressly teach that the system solves problems of observability and controllability, due to constraints stemming from the protection of proprietary data. **RO** teaches that the system solves problems of observability and controllability, due to constraints stemming from the protection of proprietary data (Abstract; Col 7, Lines 22-34), as the design can be simulated and reviewed in schematic diagram form and simulation results displayed immediately adjacent the signal lines and the design rule violations can be used to help the user identify and appropriately correct problems in the design (Abstract). It would have been obvious to one of ordinary skill in the art

at the time of Applicant's invention to modify the computer based system of **KI** with the computer based system of **RO** that included the system solving problems of observability and controllability, due to constraints stemming from the protection of proprietary data, as the design could be simulated and reviewed in schematic diagram form and simulation results displayed immediately adjacent the signal lines and the design rule violations could be used to help the user identify and appropriately correct problems in the design.

9.4 As per Claim 5, **KI, RO** and **KO** teach the system of Claim 4. **KI** and **KO** do not expressly teach that the solution to the problems of observability and controllability, is to develop an accurate customized behavioral model. **RO** teaches that the solution to the problems of observability and controllability, is to develop an accurate customized behavioral model (Abstract; Col 7, Lines 22-34), as behavioral models provide simplified model of extremely complicated devices (Col 4, Lines 19-21) and a very complete and accurate description of performance of the modeled device (Col 4, Lines 29-31). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** and **KO** with the computer based system of **RO** that included the solution to the problems of observability and controllability having an accurate customized behavioral model, as behavioral models would provide simplified model of extremely complicated devices and a very complete and accurate description of performance of the modeled device.

KI does not expressly teach the model offering sufficient parameters which can be programmed to represent framers of different vendors. **KO** teaches the model offering sufficient parameters which can be programmed to represent framers of different vendors (Page 1834,

Table 1), as the framer parameters vary for different framers from vendors (Page 1834, Table 1) and the simulation models provide for calling predefined procedures supplying various parameters (**KI**: Page 26, Col 1, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** with the computer based system of **KO** that included the model offering sufficient parameters which could be programmed to represent framers of different vendors, as the framer parameters vary for different framers from vendors and the simulation models provide for calling predefined procedures supplying various parameters.

9.5 As per claim 7, **KI** teaches a computer based method employing a customizable simulation model of an ATM/SONET framer, for system level verification and performance characterization (Page 25, Col 1, Para 2 and 3; Fig. 1; Page 26, Col 1, Para 4).

KI teaches the computer based method comprising the step of developing an accurate customizable model that offers sufficient parameters which can be programmed to represent framers from different vendors (Page 26, Col 1, Para 3). **KI** does not expressly teach the computer based method comprising the step of developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent framers from different vendor. **RO** teaches the computer based method comprising the step of developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent framers from different vendor (Abstract; Col 7, Lines 22-34), as behavioral models provide simplified model of extremely complicated devices (Col 4, Lines 19-21) and a very complete and accurate description of performance of the modeled device (Col 4,

Lines 29-31). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based method of **KI** with the computer based method of **RO** that included the step of developing an accurate customizable behavioral model that offer sufficient parameters which could be programmed to represent framers from different vendor, as behavioral models would provide simplified model of extremely complicated devices and a very complete and accurate description of performance of the modeled device.

KI does not expressly teach the computer based method comprising the step of providing two independently configurable components, a receiver and a transmitter which provide for testing with Framers from multiple vendors, by changing programmable parameters of the model. **KO** teaches the computer based method comprising the step of providing two independently configurable components, a receiver and a transmitter which provide for testing with Framers from multiple vendors, by changing programmable parameters of the model (Fig. 1; Table 1), as all communications between the ATM and the SONET have a transmit path and a receive path (Page 1833,Col 1, Para 2 and 4). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based method of **KI** with the computer based method of **KO** that included the computer based method comprising the step of providing two independently configurable components, a receiver and a transmitter which provide for testing with Framers from multiple vendors, by changing programmable parameters of the model, as all communications between the ATM and the SONET have a transmit path and a receive path.

9.6 As per claims 9, 10 and 11, these are rejected based on the same reasoning as claims 3, 4 and 5, supra. Claims 9, 10 and 11are computer based method claims reciting the same limitations as claims 3, 4 and 5, as taught throughout by **KI, RO** and **KO.**

10. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kim et al (KI)** (IEEE, August 1999) in view of **Rostoker et al. (RO)** (U.S. Patent 6,470,482) and **Koziotis et al. (KO)** (IEEE, October 1999), and further in view of **Bagheri et al. (BA)** (IEEE, May 1995).

10.1 As per Claim 2, **KI, RO** and **KO** teach the system of Claim 1. **KI** teaches the ATM/SONET framer provides one receiver and one transmitter interface to the network at a SONET line rate of 155.52 Mbps(OC-3), 622.08 Mbps(OC-12) (Page 25, Col 1, Para 3; Fig.1; Page 25, Col 2, Para 2 and 3).

KI, RO and **KO** do not expressly teach that the ATM/SONET framer provides one receiver and one transmitter interface to the network at a SONET line rate of 2488.32 Mbps(OC-48). **BA** teaches that the ATM/SONET framer provides one receiver and one transmitter interface to the network at a SONET line rate of 2488.32 Mbps (OC-48) (Page 427, Col 1, Para 2), as SONET multiplexers are capable of multiplexing information at 2488.32 Mbps due to recent advances in high speed electronics and light wave systems (Page 427, Col 1, Para 2). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI, RO** and **KO** with the computer based system of **BA** that included the ATM/SONET framer providing one receiver and one transmitter

interface to the network at a SONET line rate of 2488.32 Mbps (OC-48), as SONET multiplexers are capable of multiplexing information at 2488.32 Mbps due to recent advances in high speed electronics and light wave systems.

10.2 As per claim 8, it is rejected based on the same reasoning as claim 2, supra. Claim 8 is computer based method claim reciting the same limitations as claim 2, as taught throughout by **KI, RO, KO** and **BA.**

11. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kim et al (KI)** (IEEE, August 1999) in view of **Rostoker et al. (RO)** (U.S. Patent 6,470,482), **Koziotis et al. (KO)** (IEEE, October 1999), and **Bagheri et al. (BA)** (IEEE, May 1995), and further in view of **Zwan et al. (ZW)** (U.S. Patent 5,991,270), **Vogel (VO)** (U.S. Patent 6,075,788), and **Platt (PL)** (U.S. Patent 5,802,073).

11.1 As per Claim 6, **KI, RO** and **KO** teach the system of Claim 4. **KI** teaches the system offers programmability features of delays associated with clock domain synchronization (Page 25, Col 2, Para 4 page 26, Col 1, Para 1).

KI teaches the computer based system offers programmability and rich feature set (Page 26, Col 1, Para 3). **KI** and **RO** do not expressly teach the computer based system offers two independently configurable models, one each for the transmit side and the receive side. **KO** teaches the computer based system offers two independently configurable models, one each for the transmit side and the receive side (Fig. 1; Table 1), as all communications between the ATM

and the SONET have a transmit path and a receive path (Page 1833,Col 1, Para 2 and 4). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** and **RO** with the computer based system of **KO** that offered two independently configurable models, one each for the transmit side and the receive side, as all communications between the ATM and the SONET have a transmit path and a receive path.

KI and **RO** do not expressly teach that the computer based system offers programmability features of SONET line rates (OC-Nc: N=1 48; OC-1=51.48 Mbps). **ZW** teaches that the computer based system offers programmability features of SONET line rates (OC-Nc: N=1 48; OC-1=51.48 Mbps) (Col 1, Lines 35-41 and Col 6, Lines 30-40), as it is desirable to produce a test device that can fully test and evaluate each of these formats within a single platform (Col 1, Lines 35-41). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** and **RO** with the computer based system of **ZW** that offered programmability features of SONET line rates (OC-Nc: N=1 48; OC-1=51.48 Mbps), as it would be desirable to produce a test device that can fully test and evaluate each of these formats within a single platform.

KI and **RO** do not expressly teach that the computer based system offers programmability features of percentage of data bytes vs. overhead bytes per row. **BA** teaches that the computer based system offers programmability features of percentage of data bytes vs. overhead bytes per row (Page 427, Col 2, Para 2; Fig. 1), as the frame format varies for various STS levels ((Page 427, Col 2, Para 2). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** and **RO** with

the computer based system of **BA** that offered programmability features of percentage of data bytes vs. overhead bytes per row, the frame format varies for various STS levels.

KI and **RO** do not expressly teach that the computer based system offers programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update. **KO** teaches that the computer based system offers programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update (Page 1833,Col 1, Para 2; Col 2, Para 1 Page 1834,Col 1, Table 1), as that allows burst read and write independently of external speed and the FIFO provide for speed adaptation and minimize the latency (**KI:** Page 25,Col 2, Para4 to Page 26, Col 1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** and **RO** with the computer based system of **KO** that offered programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update, as that would allow burst read and write independently of external speed and the FIFO would provide for speed adaptation and minimize the latency.

KI and **RO** do not expressly teach that the computer based system offers programmability features of UTOPIA Level-2/3. **VO** teaches that the computer based system offers programmability features of UTOPIA Level-2/3 (Col 5, Lines 59-64), as ATM Forum specifies those standards (Col 5, Lines 59-64). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI**

and **RO** with the computer based system of **KO** that offered programmability features of UTOPIA Level-2/3, as ATM Forum specifies those standards.

KI and **RO** do not expressly teach that the computer based system offers programmability features of built-in performance checking. **VO** teaches that the computer based system offers programmability features of built-in performance checking (Abstract; Fig. 1A; Col 1, Line 65 to Col 2, Line 1), as built-in test logic can be used to achieve a high percentage of fault coverage for the whole chip (Col 1, Lines 57-59). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer based system of **KI** and **RO** with the computer based system of **KO** that offered programmability features of built-in performance checking, as built-in test logic can be used to achieve a high percentage of fault coverage for the whole chip.

11.2 As per claim 12, it is rejected based on the same reasoning as claim 6, supra. Claim 12 is computer based method claim reciting the same limitations as claim 6, as taught throughout by **KI, RO, KO, BA, ZW, VO** and **PL.**

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents and papers are cited to further show the state of the art with respect ATM/SONET (SDH) framers, their design variations and their simulation.

1. Kim et al., "Design and simulation of three ATM ASICs", The first IEEE Asia Pacific conference on ASICs, August 1999.

2. Bagheri et al., "10 Gb/s framer/demultiplexer IC for SONET STS-192 applications", Proceedings of the IEEE 1995 Custom integrated circuits conference, May 1995.

3. Koziotis et al., "0.6/spl mu/m CMOS, 622/155 mbit/s ATM-SDH/SONET framer IC", IEEE, Electronics letters, October 1999.

4. Johnston et al., "The ATM chip layer: an ASIC for B-ISDN applications", IEEE Journal on Selected areas in communications, June 1991.

5. Vogel, "SONET physical layer device having ATM and PPP interfaces", U.S. Patent 6,075,788, June 2000.

6. Rostoker et al., "Method and system for creating ... and validating structural description of electronic system from higher level behavior oriented description...", U.S. Patent 6,470,482, October 2002.

7. Zwan et al., "Dynamic communication line analyzer apparatus and method", U.S. Patent 5,991,270, November 1999.

8. Platt, "Built-in self test functional system block for UTOPIA interface", U.S. Patent 5,802,073, September 1998.

9. Rostoker et al., "Network Architecture", U.S. Patent 6,026,088, February 2000.

10. Cohoe et al., "SONET network element simulator", U.S. Patent 6,108,309, August 2000.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-73210.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
December 13, 2002

Samuel Broda

SAMUEL BRODA, ESQ.
PATENT EXAMINER